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**Service Mode
For Digital Command Control,
All Scales**

July 2012

S 9.2.3

A: Introduction

The NMRA Standards and Recommended Practices for Digital Command Control (DCC) define two modes of Digital Decoder operation: Operations Mode and Service Mode. This STANDARD describes Service Mode. The purpose of Service Mode is to allow customization and testing of Digital Decoders.

B Service Mode Environment

Given that Service Mode is designed for testing and customization of Digital Decoders, it is recommended that:

- 1) Service Mode operations should occur on an isolated section of track,
- 2) External locomotive loads (i.e. smoke generator, constant lighting, sound generators) should be switched off during programming operations. Decoders should switch off all external loads connected to the decoder upon entering service mode.
- 3) Service Mode operations should be performed in an environment with limited energy to prevent damage to decoders during programming. For the purposes of this STANDARD, limited energy is defined as 250 mA, sustained for more than 100 ms. A programmer may further limit the energy via a current limiting resistor, if it is clearly documented that not all compatible DCC devices may be programmed by this programmer.

A Programmer is the device used to create these conditions, and may be incorporated within or separate from the system Digital Command Station.

C: Digital Decoder Entry to and Exit from Service Mode

A Digital Decoder will only act on service mode instruction packets while in service mode.

A Digital Decoder will enter service mode upon receipt of a valid service mode instruction packet immediately preceded by a reset packet.

A Digital Decoder will exit service mode but not enter operations mode when any of the following conditions are true:

- 1) The Digital Decoder successfully receives a non service mode instruction packet.
- 2) 20 milliseconds have occurred since the last valid reset or service mode instruction packet was received.

Once a Digital Decoder has exited service mode, it will only re-enter operations mode upon receipt of a valid operations mode packet that is not identical to a service mode packet. This is to ensure that the decoder does not start executing service mode instruction packets as operations mode packets (Service Mode instruction packets have a short address in the range of 112 to 127 decimal.)

D: Decoder Acknowledgment Mechanism

Service Mode operations provide for an acknowledgment mechanism from the decoder to the command station/programmer. Acknowledgment refers to the ability of the Digital Decoder to respond to a Service Mode instruction issued by a Programmer. Service Mode instructions can be executed regardless of whether or not the acknowledgment mechanism is detected by the command station/programmer.

Two Acknowledgment mechanisms are available:

- Basic Acknowledgment
- Advanced Acknowledgment

45 Digital Decoders may provide either form of acknowledgment.

Basic Acknowledgment

Basic acknowledgment is defined by the Digital Decoder providing an increased load (positive-delta) on the programming track of at least 60 mA for 6 ms +/- 1 ms. It is permissible to provide this increased load by applying power to the motor or other similar device controlled by the Digital Decoder.

50 Advanced Acknowledgment

See-S-9.3.1 and S-9.3.2.

General Acknowledgment timing

For either type of Acknowledgment, if a Service Mode Write is being performed, Acknowledgment pulse(s) should not occur from the decoder until internal updating of all affected non-volatile data storage is complete in the decoder. During Service Mode the Programmer should scan for any Acknowledgment current pulse(s) in the Acknowledgment time window starting at the Packet End bit of the second service mode instruction packet and extending through the required number of instruction packets and in the case of write operations through the specified decoder-recovery-time A Command Station/Programmer may not stop sending packets to the programming track (which turns off power to the decoder) until the end of the Decoder-Recovery-Time.

60 E: Service Mode Instruction Packets

Service Mode supports four different methods for access to Configuration Variables (CVs): Direct Configuration, Address-Only, Physical Register, and Paged Addressing. The Service Mode instruction packet sequences are defined from a Command Station/Programmer perspective. A Digital Decoder must not execute any Verify or Write operations (as specified herein) unless it is in service mode (see section C) and has received two identical Service Mode packets without any intervening valid packets. Digital Decoder's must successfully perform the desired programming operation (including performing its acknowledgment function if required) within the time frame defined by this packet sequence.

Definitions

70 Within this STANDARD, bits are numbered from right to left with bit 0 (the right most bit) being the least significant bit (LSB) and bit 7 (the left most bit) being the most significant bit (MSB). Bits will be defined using the following abbreviations:

0	bit with a value of "0"
1	bit with a value of "1"
A	the configuration variable address
C	instruction type
K	instruction type
R	register number
B	position of bit
D	data value to be read or written
E	error detection bit ¹
[]	sequences between braces may be repeated, and nested one or more times as needed

75 **Long Preamble** - In Service Mode the Command Station/Programmer will increase the preamble of the packet from the minimum (per S9.2) to at least 20 bits to allow extra time for the Digital Decoder to process the packets. This is designated as "long-preamble" in the packet descriptions within this RP.

Power-On Cycle - Upon applying power to the track, the Command Station/Programmer must transmit at least 20 valid packets to the Digital Decoder to allow it time to stabilize internal operation before any Service Mode operations are initiated. During the initial decoder power-up sequence, a current load of greater than 250 mA

¹In both the three (3) data byte and the four (4) data byte packets, the last data byte of a Service Mode packet is used for error detection purposes (see RP-9.2.1 for details).

80 sustained after 100 milliseconds (ms) of initiation of packet transmission should be interpreted as an over-current fault condition for the decoder being programmed. After the power-up sequence, an decoder with all outputs turned off (i.e. lamps, amplifiers, etc.) shall not draw more than 100 ma of current except for when processing an acknowledgment.

85 **Decoder Recovery Time** - Command Station/Programmer shall send the same service mode write packets or reset packets during the Decoder-Recovery-Time until the specified packet time has been met or the until the command station/programmer has received a valid acknowledgment.

Reset Packet - Herein, a reset packet is defined as a Broadcast Decoder Reset packet, valid for all decoders (see S-9.2).

90 **Hard-Reset-Cycle** - A hard reset (see RP-9.2.1), followed by 10 idle or reset packets. This sequence is used when a Command Station/Programmer desires to return the decoder to its initial predefined state.

Page-Preset-Instruction - A packet sequence sent to guarantee the contents of the page register. The instruction sequence is (long-preamble 0 01111101 0 00000001 0 01111100 1)²

Service Mode Instruction Packets for Direct Mode

95 Direct Mode service mode instruction packets support accessing Configuration Variables by their configuration variable number (see RP-9.2.2). As an example, to determine if a Digital Decoder supports Direct Configuration Variable Addressing, the Universal Command Station/Programmer should perform two bit verifies, one verify for a bit value of '0', one verify for a bit value of '1' to the most significant bit within CV #8 (Manufacturer's ID). Acknowledgment of either bit-verify indicates that the decoder fully supports all modes of Direct Configuration Variable Addressing (Verify Byte, Write Byte, & Bit Manipulation). A Command Station, Programmer, or
100 Decoder, which supports Direct Mode, must implement all three instruction-types.

The following table shows the required packet sequence for direct mode.

Packet Sequence for Command Stations/Programmers using Direct Mode	
Optional Power-On-Cycle, if needed	
[3 or more Reset Packets	
[5 or more Verify packets to a single CV 1-1023, followed by 1 or more Reset Packets, if an acknowledgement is detected]	Or 5 or more Writes to a single CV 1-1023
]	6 or more Identical Write or Reset packets (Decoder-Recovery-Time)]
Optional Power-Off	

105 Within a verify or write sequence, the Command Station/Programmer may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received or the number of packets specified to be transmitted is completed.

Instructions packets using Direct CV Addressing are 4 byte packets of the format:

110 Long-preamble 0 0111CCAA 0 AAAAAAAAA 0 DDDDDDDD 0 EEEEEEEE 1

115 The actual Configuration Variable desired is selected via the 10 bit address with the two bit address (AA) in the first data byte being the most significant bits of the CV number. The Configuration variable being addressed is the provided 10 bit address plus 1. CV #1 is defined by the address 00 00000000. A Command Station/Programmer must provide full read and write manipulation for all values of 8 bit data.

The defined values for Instruction types (CC) are:

120 CC=10 Bit Manipulation
CC=01 Verify byte
CC=11 Write byte

Type="01" VERIFY CV BYTE

² This instruction may not have the desired effect with all older accessory decoders.

125 The contents of the Configuration Variable as indicated by the 10 bit address are compared with the data byte (DDDDDDDD). If the values are identical the Digital Decoder shall respond with an acknowledgment as defined in Section D.

Type="11" WRITE CV BYTE

The contents of the Configuration Variable as indicated by the 10 bit address are replaced by the data byte (DDDDDDDD). Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section D.

130 Type="10" CV BIT MANIPULATION

The Bit Manipulation instructions in Direct Addressing mode use a special format for the data byte DDDDDDDD:

long-preamble 0 011110AA 0 AAAAAAAA 0 111KDBBB 0 EEEEEEEE 1

135 Where BBB represents the bit position within the CV (000 being defined as bit 0), and D contains the value of the bit to be verified or written, K=1 signifies a "Write Bit" operation and K=0 signifies a "Bit Verify" operation.

140 Each bit manipulation instruction operates in a manner similar to the VERIFY CV BYTE and WRITE CV BYTE instructions (but operates on a single bit within the CV). Using the same criteria as the VERIFY CV BYTE or WRITE CV BYTE instructions, an acknowledgment will be generated in response to a VERIFY BIT or WRITE BIT instruction if appropriate.

Service Mode Instruction Packets for Address-Only Mode

145 Address-only service mode instruction packets support access to Configuration Variable #1, the Digital Decoder's short address. When a new short address (CV #1) is written using any method, a decoder must reset the extended addressing bit in the Configuration Register (CV #29) to have a value of '0', and clear the consist address (CV #19).

The following table shows the packet sequence.

Packet Sequence for Command Stations/Programmers using Address-only mode	
Optional Power-On-Cycle, if needed	
3 or more Reset Packets	
5 or more Page-Preset-packets	
6 or more Page Preset or Reset packets (Decoder-Recovery-Time from write to Page Register)	
Optional Power Off Followed by Power-On-Cycle	
[3 or more Reset Packets	
[5 or more Verifies to CV #1]	or 5 or more Writes to CV #1
]	10 or more identical Write or Reset packets (Decoder-Recovery-Time]
Optional Power Off	

150 Within a verify or write sequence, the Command Station/Programmer may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received or the number of packets specified to be transmitted is completed.

Instructions packets using Address-Only Mode are 3 byte packets of the format:

155 long-preamble 0 0111C000 0 0DDDDDDD 0 EEEEEEEE 1

In Address-Only Mode two (2) Instruction Types (C) are defined. These are:

- C=0 Verify Address
- 160 C=1 Write Address

Type="0" VERIFY ADDRESS CONTENTS

This Instruction Type causes a VERIFY operation that shall compare the eight (8) bit data value 0DDDDDDD with the contents of CV 1, the Address. If these two values are equal, the Digital Decoder shall generate an acknowledgment as defined in section D.

165 Type="1" WRITE ADDRESS CONTENTS

This Instruction Type causes a WRITE operation that shall store the eight (8) bit data value 0DDDDDDD into CV #1, the Address. Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section D.

Service Mode Instruction Packets for Physical Register Addressing

170 Physical Register addressing supports access to a limited number of Configuration Variables by using the internal “Registers” of a decoder. The following table shows the packet sequence.

Packet Sequence for Command Stations/Programmers using Physical Register Addressing	
Optional Power-On-Cycle, if needed	
3 or more Reset Packets	
5 or more Page-Pre-set-packets	
6 or more reset packets (Decoder Recovery Time from write to Page Register)	
[Optional Power-Off Followed by Power-On-Cycle ³	
[3 or more Reset Packets	
[7 or more Verifies to a specific Register]	or 5 or more Writes to a specific Register
]]	6 or more identical Writes or Reset packets (Decoder Recovery Time from write to Register)]]
Note: The Decoder Recovery Time is 10 packets long after a write to Register 1 (see Address-Only mode).	
Optional Power-Off	

175 Within a verify or write sequence, the Command Station/Programming may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received or the number of packets specified to be transmitted is completed.

Instructions packets using Physical Register Addressing are 3 byte packets of the format:

180 long-preamble 0 0111CRRR 0 DDDDDDDD 0 EEEEEEEE 1

The value encoded in bits (RRR), define one of 8 possible Physical Registers that may be read or written by a programmer. The following table maps the Physical Registers to Configuration Variables.

Register	RRR Value	CVs for Accessory Decoders	CVs for Mobile Digital Decoders
1	000	Lower Address (CV #513)	Address (CV #1)
2	001	Undefined, see Mfg. Documentation	Start Voltage (CV #2)
3	010	Undefined, see Mfg. Documentation	Acceleration (CV #3)
4	011	Undefined, see Mfg. Documentation	Deceleration (CV #4)
5	100	Undefined, see Mfg. Documentation	Basic Configuration Register (CV #29) ⁴
6	101	Undefined, see Mfg. Documentation	(Reserved for Page Register)
7	110	Version Number (CV #7)	Version Number (CV #7)
8	111	Manufacturer ID (CV #520)	Manufacturer ID Number (CV #8)

185 It is recommended that a Command Station/Programmer provide full read and write access to the 8 Physical registers (000) to (111) for all values of 8 bit data. This allows a user to directly manipulate Physical registers 1 (000) to 8 (111) and CV data in any manner. The Command Station/Programmer documentation should indicate the numbering or name scheme in use, and how these correspond to the 8 Physical Registers.

³ Some older decoders require a power off/on cycle at this point in order to be programmed. Power cycling at this point is not allowed if you are in the middle of a paged operation (see Service Mode Instruction Packets for Paged CV Addressing for more information.)

⁴ For compatibility with older systems, Register 5 may be used for other programming purposes when the Page Register is not equal to 1. If Register 5 is used in a different manner, one should restore Register 5 after the page register is reset to one. This preserves compatibility with existing decoders.

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In Physical Register Addressing Mode two (2) Instruction Types (C) are defined. These are:

C=0 Verify register/CV contents

C=1 Write register/CV contents

Type="0" VERIFY REGISTER CONTENTS

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This Instruction Type causes a VERIFY operation that shall compare the eight (8) bit data value DDDDDDDD with the contents of the specified three (3) bit register address RRR. If these two values are equal, the Digital Decoder shall generate an acknowledgment as defined in section D.

Type="1" WRITE REGISTER CONTENTS

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This Instruction Type causes a WRITE operation that shall store the eight (8) bit data value DDDDDDDD into one of the eight registers as specified by the three (3) bit register address RRR. Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section D.

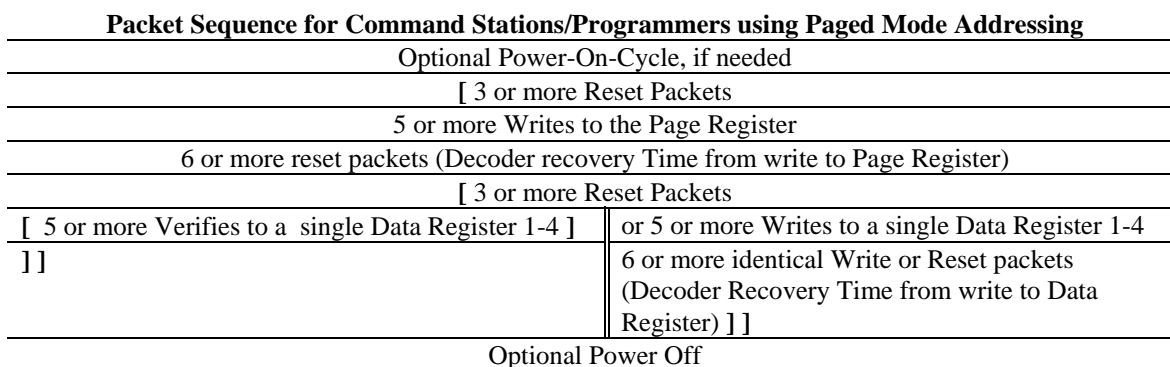
Service Mode Instruction Packets for Paged CV Addressing:

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Implementations that require access to a larger number of Configuration Variables than possible using just the 8 Physical Registers, can use an extended 3 byte programming format called Paged CV addressing. If a decoder does not implement Paged CV addressing, it must not respond to Paged CV programming commands when the page register has a value greater than 1.

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Paged CV Addressing, implements access to all 1024 Configuration Variables through advanced usage of the 8 Physical "registers" or storage locations. The first four registers are used as Data Registers on a particular page. The sixth register holds the current page number. The following diagram shows the order of packet sequences for paged mode:



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Within a verify or write sequence, the Command Station/Programming may cease sending packets and continue with the next step in the sequence when either a decoder acknowledgment is successfully received or the number of packets specified to be transmitted is completed.

Instructions packets using Paged Mode programming are 3 byte packets of the format:

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long-preamble 0 0111CRRR 0 DDDDDDDD 0 EEEEEEEE 1

It is recommended that a Command Station/Programmer provide full read and write manipulation for all values of 8 bit data.

225

The five (5) additional Physical registers, defined by (RRR), in use for Paged CV Addressing are:

Register	RRR Value	
1	000	Data Register 0
2	001	Data Register 1
3	010	Data Register 2
4	011	Data Register 3
5	100	Basic Configuration Register ⁵
6	101	Paging Register

230 -1 through 4 (000-011) are DATA REGISTERS. They point to a set of 4 Configuration Variables as determined by
the contents of the PAGING REGISTER. Register 0 points to the first CV in the set while Register 3
points to the last CV in the set.

235 -5 (100) is the BASIC CONFIGURATION REGISTER. This register defines the basic configuration of the Digital
Decoder. See the definition of Configuration Variable 29 (RP-9.2.2) for further information on the
contents of this register in a Multi-function Digital Decoder and see Configuration Variable 541 (RP-
9.2.2) for further information on the contents of this register in an Accessory Decoder.

240 -6 (101) the PAGING REGISTER. This register is used as an offset for the DATA REGISTERS to allow access to
the larger set of 1024 configuration variables. The default value for this register is 1

To Calculate the CV number referred to by a Data register and Page Register value:

(1) Subtract 1 from the value in the Page Register. Then multiply this value by 4.

(2) Add the number of the Data Register (000-011 or 0-3 decimal) to step (1)

(3) Add 1 to result of step (2) and this is the number of the CV being accessed.

245 The inverse of this sequence can be used to calculate the Page number and Data register for a particular CV
number.

For Example: To find the Page Register and Data Register for CV 65 - Kick Start;

$$\text{CV \#65} - 1 = 64$$

$$64 \text{ divided by } 4 = 16, 0 \text{ remainder.}$$

$$16 + 1 = 17$$

250 Page Register 17; Data Register 0

Registers 5, 7 and 8 are unaffected by the contents of the Page Register value (see Service Mode Instruction Packets
for Physical Register Addressing for more information)

In Paged CV Addressing Mode two (2) Instruction Types (C) are defined. These are:

255 C=0 Verify register/CV contents

C=1 Write register/CV contents

Type="0" VERIFY REGISTER/CV CONTENTS

260 This Instruction Type causes a VERIFY operation that shall compare the eight (8) bit data value DDDDDDDD
with the contents of the specified three (3) bit register address RRR. If these two values are equal, the Digital
Decoder shall generate an acknowledgment as defined in section D.

When the Register address is in the Data Register range of (000) to (011), the stored value of the CV referenced
by the Data Register in combination with the Page register value will be verified.

Type="1" WRITE REGISTER/CV CONTENTS

⁵ Refer to the section on Physical Register addressing for other compatibility issues with the use of this register.

265 This Instruction Type causes a WRITE operation that shall store the eight (8) bit data value DDDDDDDD into one of the eight registers as specified by the three (3) bit register address RRR. Upon completion of all write operations, the Digital Decoder may respond with an acknowledgment as defined in Section D.

When the Register address is in the Data Register range of (000) to (011), the CV referenced by the Data register in combination with the Page register value will be written.

270 If the decoder maintains an internal Page Register copy that is only valid when power is applied, it should NOT be initialized when a Reset packet is received. This ensures a Programmer can load the Page Register in a decoder and follow this with multiple Write and/or Verify operations while power and packets remain on.

275 To ensure compatibility with earlier Command Station/Programmers, a Command Station/Programmer should set the Page Register (101) to 'Page 1' (a data value of 1) at the end of programming. It is also recommended that decoders provide a mechanism to automatically reset their page registers to have a value of 1 after programming is completed. (See Section C: Entry to and Exit from Service Mode)

Decoder Factory Reset

280 From time to time it may necessary to request that the decoder reprogram all its CVs to a factory default condition. The following command sequence⁶ shall be used for this purpose. The packet sequence for this command is identical to the packet sequence specified for Service Mode Instruction Packets for Physical Register Addressing. The instruction packets for Decoder Factory Reset are 3 byte packets of the format:

285 long-preamble 0 01111111 0 00001000 0 01110111 1

290 This Instruction Type causes a WRITE operation that instructs the decoder to return to a factory default condition. Because the packet sequence in service mode provides insufficient time for the decoder to rewrite all its CVs, the actual reprogramming all the decoder's CVs will normally occur during each subsequent power on cycle until such time that all CVs have been returned to a factory default condition. A value of 255 will be placed in CV8 until such time that the decoder has successfully rewritten all CVs to their factory default condition.

F: Methods of Programming Required

295 To conform to this STANDARD, Command Station or Programmers must implement one of the following groups of programming methods. The manufacturer must clearly label, using the defined terms below, which form(s) of programming are supported.

Command Station or Programmers

Address-Only Programmers	program CV #1 via Address-Only Mode
Register-Mode CV Programmers	Program a selected subset of CVs via Physical Register, subset must include CV #1 using Address Only Mode and be clearly defined and documented
Paged CV Programmers	Program a selected sub-set of CVs via Physical Register and Paged Addressing. Subset must include CV #1 using Address Only Mode and be clearly defined and documented.
Direct CV Programmers	Program a selected subset of CVs via Physical Register and Direct Addressing, subset must include CV #1 in Address-Only Mode, and be clearly defined and documented.
Universal CV Programmers	Have the ability to read and write a subset of CVs via Direct, Physical Register and Paged Addressing. Subset must include CV #1 using Address Only Mode and be clearly defined and documented.

300 Effective 1-Aug-2002 all Command Stations or Programmers submitted for Conformance must implement Direct Mode.

⁶ Several valid existing alternative means for achieving decoder factory reset are also in use. Manufacturers may continue to use these alternate means for performing factory decoder reset but are required to also support the standard specified means in new designs for achieving this result.

For complete backward compatibility with decoders that were produced prior to 1-Aug-2002 which do not support direct mode, support for paged mode is strongly encouraged.

Decoders

305 All programmable decoders must perform Address-Only mode, and either Physical Register or Paged Addressing as appropriate. Decoders that support Service Mode programming for more CVs than Physical Register mode can support, and are submitted for Conformance after 1-Aug-2002, must support Direct Mode. If the decoder supports Direct CV Addressing, the decoder also needs to support Address-Only programming. The manufacturer must clearly label, using the terms described in this RP, which form(s) of programming are supported.

310 For complete backward compatibility with Command Stations or Programmers that were produced prior to 1-Aug-2002 which do not support direct mode, support for paged mode is strongly encouraged.

APPENDIX A: Address Query Instruction

315 The Address Query instruction is used in older Digital Decoders to verify a specific decoder address, CV #1. The format of the instruction is:

```
long-preamble 0 AAAAAAAAA 0 11111001 0 EEEEEEEE 1
```

320 If the address in the packet matches the address of the Digital Decoder, the Digital Decoder generates an acknowledgment as specified in Section D. This instruction is included to allow Programmers to verify addresses of older decoders. It is recommended that a Programmer first attempt to read CV# 1 with the Direct or Paged verify mechanism before invoking this method of Address Query. After unsuccessfully attempting to read the value of CV# 1, it can be verified to match the address of the Decoder using this Address Query command. This Address Query Instruction may only be issued for the Address range of AAAAAAAAA from 1 to 111 decimal.

325 APPENDIX B: Service Mode Decoder Lock Instruction

This Appendix contains the definition of an additional instruction. A DCC product need no implement the feature described in this Appendix, but if it is implemented, it must be implemented completely.

330 Additional information is available in Technical Note TN-2-05.

335 The Service Mode Decoder Lock instruction prevents service mode programming of some decoders, while allowing programming of others on a single track. Note: This is not a substitute for a low current programming track for new decoder instructions. Command stations/programmers must contain clear instructions on how to install and utilize a low current programming track.

The format of the instruction is:

```
long-preamble 0 00000000 0 11111001 0 0aaaaaaa 0 EEEEEEEE 1
```

340 Where "aaaaaaa" is the short address of the decoder that will continue to execute service mode commands.

345 Upon receiving a 0xF9 Service Mode Decoder Lock instruction, a decoder which implements this feature will check its address against the short address contained in the packet ("aaaaaaa"). If its address does not match the address in the packet, the decoder will be considered locked and will ignore all subsequent service mode instructions (even after a power cycle).

350 To unlock a decoder that has been locked using the Service Mode Decoder Lock instruction, the decoder must receive a valid NMRA DCC packet other than either a valid service mode packet or a valid Service Mode Decoder Lock instruction (with an "aaaaaaa" that does not match it address). Once unlocked, the decoder will accept all subsequent service mode packets.